



DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	WO 00 39669 A (INTEL CORP) 6 July 2000 (2000-07-06)	1,2,5	G06F9/38
Y	* page 3, line 23 - line 32 * * page 4, line 6 - line 28 * * page 5, line 29 - line 31 *	3,4	
Y	YOSHIDA T ET AL: "A strategy for avoiding pipeline interlock delays in a microprocessor" PROCEEDINGS OF THE INTERNATIONAL CONFERENCE ON COMPUTER DESIGN: VLSI IN COMPUTERS AND PROCESSORS. CAMBRIDGE, MA., SEPT. 17 - 19, 1990, LOS ALAMITOS, IEE COMP. SOC. PRESS, US, 17 September 1990 (1990-09-17), pages 14-19, XP010020910 ISBN: 0-8186-2079-X * page 2, column 2, paragraph 3 - page 3, column 1, paragraph 3 *	3,4	
A	US 5 185 868 A (TRAN THANG M) 9 February 1993 (1993-02-09) * column 4, line 11 - line 19 *	1,2,5	TECHNICAL FIELDS SEARCHED (Int.Cl.7) G06F
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 31 July 2003	Examiner Moraiti, M
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document			
T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 03 09 0089

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

31-07-2003

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